UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,020	04/01/2004	Darius D. Gaskins	CNTR.2207	2625

23669 7590 09/28/2006

HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
PATEL, ANAND B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,020	GASKINS ET AL.	
	Examiner	Art Unit	
	Anand Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,14 and 17-20* is/are rejected.

7)☒ Claim(s) *10,13,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: paragraph 2 does not contain the serial number of the copending application.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-4, 8, 11-12, 14, 17-20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 10-11, 15-18, 20 of copending Application No. 10/816004. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application contains every limitation of the claims in the instant application.

- Claim 1 claims the same invention as claim 1 of the copending application.
- Claim 2 claims the same invention as claim 3 of the copending application.
- Claim 3 claims the same invention as claim 4 of the copending application.

- Claim 4 claims the same invention as claim 2 of the copending application.
- Claim 8 claims the same invention as claim 10 of the copending application.
- Claim 11 claims the same invention as claim 11 of the copending application.
- Claim 12 claims the same invention as claim 11 of the copending application.
- Claim 14 claims the same invention as claim 15 of the copending application.
- Claim 17 claims the same invention as claim 16 of the copending application.
- Claim 18 claims the same invention as claim 17 of the copending application.
- Claim 19 claims the same invention as claim 18 of the copending application.
- Claim 20 claims the same invention as claim 20 of the copending application.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5-7, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6259293 to Hayase et al (Hayase) in view of Applicant's Admitted Prior Art (AAPA).

- As per claim 1, Hayase discloses a power management controller for instantaneous frequency-based microprocessor power management, comprising:
  - A first PLL (top PLL, 9) that generates a first core source clock signal at a first frequency based on a signal (figure 14);

- A second PLL (middle PLL, 9) that generates a second core source clock signal at a frequency based on a signal (figure 14);
- Select logic (10) that selects between said first and second core source clock signals to provide a core clock signal for the microprocessor based on a select signal (column 2, lines 13-20; inherent that 10 has a select signal input); and

Hayase fails to disclose specifics about the PLLs and source control logic. AAPA teaches:

- A programmable PLL (105) that generates a clock signal at a programmable frequency (paragraphs 5-6) based on a frequency control signal (CORERATIO) and a bus clock signal (BUS CLOCK);
- Source control logic (103) that detects power conditions via at least one power sense signal (101), that provides said frequency control signal according to said power conditions (figure 1).

An advantage of the system taught by AAPA is the ability to lower power in the system (paragraph 6). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase with the clock control logic as taught by AAPA. Motivation to modify is to cut power costs.

- As per claim 5, AAPA teaches wherein said first frequency is associated with the full operating frequency of the microprocessor (paragraph 6).
- As per claim 6, AAPA teaches wherein said second core source clock signal is programmed to a reduced frequency appropriate for reduced power conditions (paragraph 6).
- As per claim 7, AAPA teaches wherein said at least one power signal is provided by any of a plurality of mechanisms including registers, transducers and power signals (figure 1, 101).
- As per claim 14, Hayase discloses a method of instantaneous processor power management, comprising:
  - Generating a first source clock at a first frequency based on a clock (figure 14);

- Generating a second source clock at a second frequency based on a clock and an input (figure 14);
- Switching between the first and second source clock signals (column 2, lines 13-20).

AAPA teaches:

- Sensing power conditions (101); and
- A PLL generating a clock at a full power frequency and at a reduced power frequency (paragraph 6).

6. Claims 2, 8-9, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayase in view of AAPA and US Patent No 7019577 to Agrawal et al (Agrawal).

- As per claim 2, Hayase and AAPA fail to disclose a lock signal. Agrawal teaches wherein the PLL generates a lock signal when said clock signal is at a frequency indicated by said frequency control signal (column 4, lines 45-46). An advantage of the system taught by Agrawal is the ability to improve clock generation techniques (column 1, lines 23-31). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Hayase and AAPA with the lock signal as taught by Agrawal. Motivation to modify is to cut costs and wasted time.
- As per claim 8, Hayase discloses a microprocessor, comprising:
  - A primary PLL (top PLL, 9) that provides said first core clock signal at a first frequency based on a signal (figure 14);
  - A PLL (middle PLL, 9) that generates a second core source clock signal at a frequency based on a signal (figure 14);
  - Select logic (10) that selects between said first and second core clock signals to provide a core clock signal based on said select signal (column 2, lines 13-20; inherent that 10 has a select signal input).

  AAPA teaches:

- A sense interface (interface receiving 101) receiving at least one power sense signal indicative of power conditions (101);
- A clock source controller (103), coupled to said sense interface (figure 1), that provides a core ratio bus indicative of a reduced core clock frequency (paragraph 6);
- A programmable PLL (105), coupled to said clock source controller (figure 1), that generates a clock signal at a programmable frequency (paragraphs 5-6) based on a frequency control signal (CORERATIO) and a bus clock signal (BUS CLOCK).

  Agrawal teaches a PLL that outputs a lock signal indicating that said core clock frequency is operative (column 4, lines 45-46).

- As per claim 9, AAPA teaches wherein said sense interface receives at least one external power sense signal (101).
- As per claim 11, AAPA teaches wherein said clock source controller determines a reduced power level sufficient to meet said power conditions, and provides said core ratio bus to indicate a core clock frequency to achieve said reduced power level (paragraphs 5-6).

Allowable Subject Matter

7. Claims 3-4, 10, 12-13, 15-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended or disclaimed to overcome the double patenting rejection above. Prior art fails to disclose or suggest wherein said source control logic controls said select signal to switch from said first core source clock signal to said second core source clock signal in response to said lock signal. Prior art also fails to disclose or suggest programming a register to indicate a reduced power level, and wherein said monitoring at least one power sense signal comprises reading the register. Prior art fails to disclose or suggest the specific method of switching, including initially selecting the first source clock

signal; providing the frequency control input based on sensed power conditions to indicate the reduced power frequency; ramping the second source clock signal to the reduced power frequency in response to the frequency control input; providing a lock indication when the second source clock signal achieves the reduced power frequency; and switching to the second source clock signal when the lock indication is provided.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on Mon-Fri 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ABP

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100